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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,997	07/17/2003	David Casey	30678-CNT1	1004

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EXAMINER	
NGUYEN, HAU H	

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	10/621,997	CASEY, DAVID	
	Examiner	Art Unit	
	Hau H Nguyen	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1, 4-6, and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Maeda et al. (U.S. Patent No. 5,968,145).

Referring to claims 1 and 4-6, Maeda et al. teach a data processing unit wherein, as shown in Fig. 1, the CPU block 12 of the three blocks includes, besides the CPU 3, the internal memory 4 (first memory) accessed only by the CPU 3, and the CPU bus 11 for connecting the CPU 3 to the internal memory 4. The DMAC block 14 includes, in addition to the DMAC 5 (DMA controller), the storage 7 (a second memory) accessed by the DMAC 5 and CPU 3, and the I/O equipment 6 (peripheral device) and DMAC bus 13 which are accessed only by the DMAC 5. The bus connecting means 15 (a selector) manages the connection state of the CPU bus 11 with the DMAC bus 13, which keeps the disconnected state unless the CPU 3 enables the access request to the storage 7 (col. 3,

lines 14-26). If the DMAC 5 has gained the right of using the DMAC bus 13 as at the point D in FIG. 2, the bus connecting means 15 connects the CPU bus 11 to the DMAC bus 13 after the DMAC 5 has relinquished the right of using the DMAC bus 13 at the E point in FIG. 2 so as not to impair the transfer function of the DMAC 5 (col. 3, lines 48-55). (Thus, a wait state is created during the DMA access to the second memory to prevent CPU accessing the second memory, and enabling the CPU access to the second memory when the DMA controller finishes reading data from the second memory). Since the disconnected state (a data bus isolation gate) between the CPU bus 11 and the DMAC bus 13 is maintained as long as the CPU 3 disables the access request to the storage 7 as described above, the CPU 3 can access the internal memory 4 independently of the transfer of the DMAC 5 (allowing CPU access to the first memory while DMA accessing the second memory) (col. 3, lines 57-62).

In regard to claim 8, as shown in Fig. 3, Maeda et al. teach the internal (first) memory and the external (second) memory can be RAM (formed on separated block of RAM) (col. 1, lines 19-25).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda et al. (U.S. Patent No. 5,968,145) in view of Kim (U.S. Patent No. 5,898,879).

Referring to claim 2, as applied to claim 1 above, Maeda et al. teach all the limitations of claim 2, except that the DMA controller creates a wait state by suppressing a clock of the CPU.

However, Kim teach a method reducing power consumption during a CPU idle condition when a bus master other than the CPU, such as a Direct Memory Access (DMA) controller or a refresh controller, uses the bus system. Power consumption is reduced by lowering or stopping a clock signal supplied to the CPU (col. 1, lines 10-15, col. 2, lines 63-67, and col. 3, lines 1-4).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Kim in combination with the method as taught by Maeda et al. in order to reduce power consumption (col. 1, lines 10-15).

5. Claims 3, 7, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda et al. (U.S. Patent No. 5,968,145) in view of Shay (U.S. Patent No. 5,900,886).

Referring to claims 3, 7, and 9, as applied to claim 1 above, Maeda et al. teach for transferring data to peripheral device (I/O equipment 6), and also teach the improvement of data transfer over a prior art microcomputer chip shown in Fig. 3. Thus, Maeda et al. teach all the limitations of claims 3, 7 and 9, except that the peripheral device including a display controller and a display, and the CPU, the second memory, the DMA controller, and the display controller are integrated on a single chip, and the first and second memory are formed on a single block of RAM partitioned into the first and second portions.

However, as shown in Fig. 1, Shay teaches an integrated circuit 37, containing a CPU 33, DMA controller 35, display controller 30, and display 32 (col. 4, lines 34-39).

Shay also teaches shared system memory 31 (single block of RAM) is partitioned into first and second portions 40 and 42 (Figs. 1 and 5, col. 6, lines 1-19).

Therefore, it would have been obvious to one skilled in the art to utilize the method of integrating functional components in an integrated circuit as taught by Shay in combination with the method of DMA controlling as taught by Maeda et al. in order to obtain better cost and board space efficiency (col. 7, lines 14-26).

6. Claims 10, 12-14, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vax (U.S. Patent No. 5,467,274) in view of Maeda et al. (U.S. Patent No. 5,968,145).

Referring to claim 10, Vax teaches a GPS receiver 2 with an antenna ANT. coupled to receive GPS signals (Fig. 4). As shown in Fig. 6A, the CPU 15 including a DMA controller is coupled to receive GPS signals through the RS-232 communication circuits 16, 17 (col. 6, lines 48-60).

Thus, Vax teaches all the limitations of claim 10, except for the DMA controller having a first and second memory, and the DMA controller capable of creating a wait state to prevent the CPU from accessing the second memory.

However, as cited above, Maeda et al. teach a data processing unit having a first memory and a second memory accessible to the CPU, and the DMA controller is operable to read data from the second memory, to create a wait state to prevent the CPU from accessing the second memory while the DMA controller is reading data from the second memory, enable the CPU accessing the second memory when the DMA controller finishes reading data from the second memory, and to allow the CPU to access the first memory while the DMA controller is reading data from the second memory.

Therefore, it would have been obvious to one skilled in the art to utilize the DMA controller as taught by Maeda et al. and incorporate into the GPS receiver as taught by Vax in order to increase the operating ratio of the CPU without giving any adverse effect on the data transfer function of the DMA controller (col. 2, lines 1-3).

In regard to claims 12-14, as cited above, although Vax does not teach a selector or an data bus isolation gate, Maeda et al. teach the bus connecting means 15 (a selector) manages the connection state of the CPU bus 11 with the DMAC bus 13, which keeps the disconnected state unless the CPU 3 enables the access request to the storage 7 (a data bus isolation gate) (col. 3, lines 23-26).

Therefore, it would have been obvious to one skilled in the art to utilize the DMA controller as taught by Maeda et al. and incorporate into the GPS receiver as taught by Vax in order to increase the operating ratio of the CPU without giving any adverse effect on the data transfer function of the DMAC (col. 2, lines 1-3).

In regard to claim 17, although Vax does not teach the first and second memories are formed on separate blocks of RAM, Maeda et al., as cited above, teach the first and second memory are formed on separate blocks of RAM.

Therefore, it would have been obvious to one skilled in the art to utilize the DMA controller as taught by Maeda et al. and incorporate into the GPS receiver as taught by Vax in order to increase the operating ratio of the CPU without giving any adverse effect on the data transfer function of the DMAC (col. 2, lines 1-3).

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vax (U.S. Patent No. 5,467,274) in view of Maeda et al. (U.S. Patent No. 5,968,145), and further in view of Kim (U.S. Patent No. 5,898,879).

Referring to claim 11, as applied to claim 10 above, Vax and Maeda et al. teach all the limitations of claim 11, except that the DMA controller creates a wait state by suppressing a clock of the CPU.

However, Kim teach a method reducing power consumption during a CPU idle condition when a bus master other than the CPU, such as a Direct Memory Access (DMA) controller or a refresh controller, uses the bus system. Power consumption is reduced by lowering or stopping a clock signal supplied to the CPU (col. 1, lines 10-15, col. 2, lines 63-67, and col. 3, lines 1-4).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Kim in combination with the method as taught by Maeda et al. in order to reduce power consumption (col. 1, lines 10-15).

8. Claims 15-16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vax (U.S. Patent No. 5,467,274) in view of Maeda et al. (U.S. Patent No. 5,968,145), and further in view of Shay (U.S. Patent No. 5,900,886).

Referring to claims 15-16, and 18, as applied to claim 10 above, Vax teaches a GPS receiver; Maeda et al. teach a method of DMA controlling transferring data when CPU accessing the second memory, and also teach the improvement of data transfer over a prior art microcomputer chip shown in Fig. 3. Thus, Maeda et al. teach all the limitations of claims 15-16, and 18, except that the peripheral device including a display controller and a display, and the CPU, the second memory, the DMA controller, and the display controller are integrated on a single chip, and the first and second memory are formed on a single block of RAM partitioned into the first and second portions.

However, as shown in Fig. 1, Shay teaches an integrated circuit 37, containing a CPU 33, DMA controller 35, display controller 30, and display 32 (col. 4, lines 34-39). Shay also teaches shared system memory 31 (single block of RAM) is partitioned into first and second portions 40 and 42 (Figs. 1 and 5, col. 6, lines 1-19).

Therefore, it would have been obvious to one skilled in the art to utilize the method of integrating functional components in an integrated circuit as taught by Shay in combination with the method of DMA controlling as taught by Maeda et al. in order to obtain better cost and board space efficiency (col. 7, lines 14-26).

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

H. Nguyen

11/17/2004

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600